Electronic Version
Stylesheet Version v1.1.1

AN IMPROVED VOLTAGE TO CURRENT CONVERTER CIRCUIT

Abstract

The improved voltage to current (V2I) converter circuit (31) is basically comprised of three stages in CMOSFET technology. The first stage (11) amplifies the input voltage signals (V_{FILTP},V_{FILTN}). The second stage (12) coupled to the first stage includes first and second/third current sources (20,21/22) loaded by respective transistors (TN1,TN2) that are connected in a current mirror configuration with a common node (23) therebetween. The third stage (13) coupled to the second stage consists of an output transistor (TN3) loaded by another transistor (TN4) to form a half cascode current mirror having its drain connected to said second/third current sources and to the output terminal (24). The gate of the output transistor is coupled to a bias voltage (V_{BN0}) and to the drain of an additional transistor (TN'), the gate of which is coupled to said common node so that the potential on the gate of the output transistor can vary to have both transistors of the third stage in the saturation state for a wide range of the current flowing through the transistors of the half cascode current mirror. The

improved V2I converter circuit is well adapted to phase locked loop (PLL) applications.